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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,513	09/23/2003	Sung Mao Wu	4459-131	2585

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EXAMINER	
NGUYEN, HOAI AN D	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,513	WU ET AL.	
	Examiner	Art Unit	
	Hoai-An D. Nguyen	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 10, 14, 15 and 22-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Buie (US 3,768,157 A) in view of Liu et al. (US 2004/0150411 A1).

Buie discloses a microcircuit package comprising:

With regard to claims 1 and 10, a substrate (FIG. 4b, base member 13), a first surface (FIG. 4b, the inner surface of the left wing of the U-shape base member 13), a second surface opposite to the first surface (FIG. 4b, the inner surface of the right wing of the U-shape base member 13) (providing an impedance standard substrate which has a first surface and a second surface opposite to the first surface), a thru-circuit (FIG. 4b, semiconductor device 10 and gold wires 21) having two contacts (FIG. 4b, fingers 16) electrically connected to each other and respectively disposed on the first surface and the second surface (providing a thru-circuit having two contacts electrically connected to each other and respectively disposed on the first surface and the second surface) (From column 2, line 59 to column 3, line 3 and from column 3, line 63 to column 4, line 11).

However, he does not explicitly teach the followings:

- The contacts are adapted to electrically connect to the two probes of the vector network analyzer, respectively (driving the two probes to be in contact with the two contacts, respectively, and sending the measuring signal).

Meanwhile, Liu et al. teach an electronic calibration circuit for calibrating a network analyzer comprising:

With regard to claims 1 and 10, an electronic calibration integrated circuit 130 coupled to port 132 and port 134 (FIG. 1). Port 132 and port 134 are configured to be coupled to the VNA, providing connection to multiple impedance states (Paragraph [0020]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the microcircuit package of Buie to incorporate the teaching of an electronic calibration integrated circuit taught by Liu et al. since Liu et al. teach that such an arrangement is beneficial to provide for a single integrated circuit having transmission lines lengths short enough to reduce interactions of impedance mismatches and to reduce transmission loss as disclosed in paragraph [0022].

In addition, Buie also discloses the followings:

With regard to claims 2 and 14, the substrate / thru-circuit comprises a via (FIG. 4b, semiconductor device 10 and gold wires 21) electrically connected to the two contacts (FIG. 4b, fingers 16).

With regard to claim 3, the two contacts are disposed by the opposite sides of the via, respectively (See FIG. 4b and look from left to right direction).

With regard to claim 4, the two contacts are disposed by the same side of the via (See FIG. 4b and look from top to bottom direction).

With regard to claims 5 and 15, a side wall defined between the first surface and the second surface (FIG. 4b, the air wall between the inner surface of the left wing of the U-shape base member 13 and the inner surface of the right wing of the U-shape base member 13), wherein the two contacts (FIG. 4b, fingers 16) of the thru-circuit (FIG. 4b, semiconductor device 10 and gold wires 21) abut the edge (the bottom of the U-shape base member 13) of the impedance standard substrate and the thru-circuit further comprises a trace (FIG. 4b, semiconductor device 10 and gold wires 21) disposed on the side wall for electrically connecting the two contacts (See FIG. 4b).

With regard to claim 6, the trace is disposed by circuit layout on the side wall (See FIG. 4b).

With regard to claims 22 and 23, the two contacts are exposed on the first and second surfaces, respectively, whereby allowing the two probes of the vector network analyzer to come into direct, electrical and physical contact with the two contacts of the substrate, respectively (driving the two probes, each of the two probes of the vector network analyzer is brought in direct, electrical and physical contact with one of the two contacts of the substrate) (See FIG. 4b).

With regard to claim 24, providing the thru-circuit (FIG. 4b, semiconductor device 10 and gold wires 21) comprising exposing the two contacts (FIG. 4b, fingers 16) of the substrate on the first and second surfaces, respectively, for allowing direct, electrical and physical contact between each of the two probes of the vector network analyzer with one of the two contacts of the substrate (See FIG. 4b).

With regard to claim 25, driving the two probes, the two probes of the vector network analyzer are simultaneously brought in direct, electrical and physical contact with the respective two contacts of the substrate (See FIG. 4b).

3. Claims 7-9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buie in view of Liu et al. as applied to claims 1 and 10 above, and further in view of Dunsmore.

Buie and Liu et al. together teach all that is claimed as discussed in the above rejection of claims 1-6, 10, 14, 15 and 22-25, but they do not explicitly teach the followings:

- A pair of open-circuits disposed on the first surface and the second surface, respectively.
- A pair of short-circuits disposed on the first surface and the second surface, respectively.
- A pair of load-circuits disposed on the first surface and the second surface, respectively.

However, Dunsmore teaches a method of calibrating a test system using unknown standards comprising:

- With regard to claims 7 and 11, a pair of open-circuits disposed on the first surface and the second surface, respectively (From column 8, line 41 to column 9, line 2 and from column 10, line 59 to column 11, line 29).
- With regard to claims 8 and 12, a pair of short-circuits disposed on the first surface and the second surface, respectively (From column 8, line 41 to column 9, line 2 and column 10, lines 26-58).

- With regard to claims 9 and 13, a pair of load-circuits disposed on the first surface and the second surface, respectively (From column 8, line 41 to column 9, line 2 and column 11, lines 30-56).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the microcircuit package of Buie and Liu et al. to incorporate the teaching of a pair of open-circuits, a pair of short-circuits and a pair of load-circuits disposed on the first surface and the second surface, respectively taught by Dunsmore since Dunsmore teaches that such an arrangement is beneficial to provide for a choice of calibration standards based on conventional guidelines for choosing standards as disclosed in column 8, lines 41-60.

Response to Arguments

4. Applicant's arguments with respect to claims 1-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant's attention is invited to the followings whose inventions disclose similar devices.

- Strid et al. (US 5,047,725 A) teach a verification and correction method for an error model for a measurement network.

- Yanagawa et al. (US 5,661,404 A) teach a circuit network measurement device and calibration method.
- Wang (US 5,760,336 A) teach a burn and explosion-resistant circuit package for a varistor chip.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

CONTACT INFORMATION

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai-An D. Nguyen whose telephone number is 571-272-2170. The examiner can normally be reached on M-F (8:00 - 5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lefkowitz can be reached on 571-272-2180. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANJAN DEB
PRIMARY EXAMINER

Hoai-An D. Nguyen
Examiner
Art Unit 2858
HADN

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